MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

DET5078 – ANALOG ELECTRONICS 2

(Diploma in Electronics Engineering)

12 MARCH 2018
9.00 AM – 11.00 AM
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This question paper consists of **6** pages with **4** questions only.
2. Attempt **ALL** questions. All necessary working steps must be shown.
3. Please write all your answers in the answer booklet provided.

QUESTION 1 [20 marks]

(a) With the aid of a proper diagram, describe how the n-type depletion type MOSFET can be turned OFF. (7 marks)

(b) Describe the advantages of the Junction Field Effect Transistor (JFET) over the Bipolar Junction Transistor (BJT). (5 marks)

(c) Define the term "Biasing" of a transistor. (2 marks)

(d) Figure 1 shows a high frequency amplifier circuit for Field Effect Transistor.

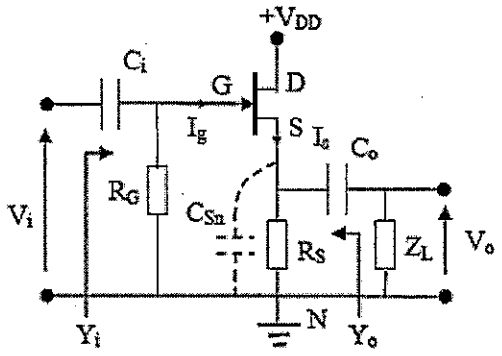

Figure 1

(i) Explain the Miller Theorem. (3 marks)

(ii) Sketch the high frequency model from Figure 1 after applying Miller's Theorem. (3 marks)

Continued ...

QUESTION 2 [20 marks]

(a) Describe **THREE (3)** types of the amplifier distortion. (6 marks)

(b) Explain a major drawback of the Class B amplifier with aid of proper diagram. (10 marks)

(c) Figure 2 shows the resulting collector current and voltage output waveforms. The overall time delay between input and output transitions is called propagation delay. Briefly describe the rise time and fall time based on the waveform. (4 marks)

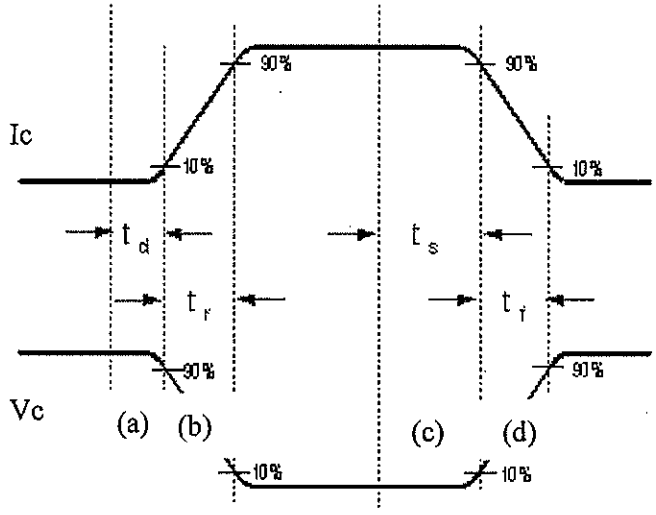

Figure 2

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QUESTION 3 [30 marks]

(a) A JFET transistor circuit is shown in Figure 3. Given $R_D = 2$ kΩ, $R_G = 1$ MΩ, $V_{DD} = 15$ V, $R_S = 750$ Ω, $I_{DSS} = 12$ mA and $V_p = -9$ V,

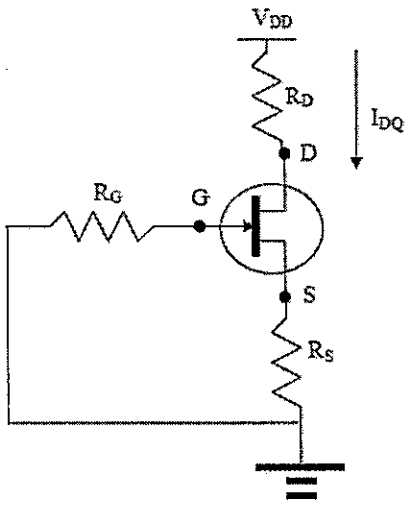

Figure 3

Determine the following:

(i) Identify the type of the biasing circuit. (1 mark)

(ii) V_{GSQ} and I_{DQ} (6 marks)

(iii) V_D, V_S and V_{DS} (6 marks)

Continued ...

(b) A JFET circuit as shown in Figure 4 operates at 30 kHz with $R_G = 1\ M\Omega$, $R_D = 125\ k\Omega$, $Z_L = 10\ k\Omega$. The transconductance is $g_m = 2$ mA/V while the internal resistance of JFET is $r_d = 50\ k\Omega$. The coupling and bypass capacitors have large values of capacitance with $C_{gs} = 3$ pF, $C_{ds} = C_{gd} = 1$ pF.

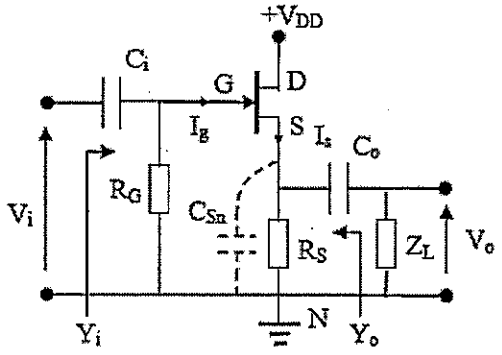

Figure 4

Determine the following:

(i) Identify the type of the circuit configuration. (1 mark)

(ii) $|A_v|$ (7 marks)

(iii) Y_A (3 marks)

(iv) $|Z_i|$ (6 marks)

Hint:

$G = 1/R$, $Y = j\omega C_s$, $g = 1/r$ $Y = 1/Z$

$Y_A = Y(1 - A_v)$, $Y_B = Y(1 - 1/A_v)$, $Y_i = G_G + Y_{gd} + Y_A$

$$A_V = \frac{g_m + Y_{gs}}{Y_{gs} + g_m + g_d + Y_{ds} + Y_{Sn} + G_S + Y_L}$$

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QUESTION 4 [30 marks]

(a) Figure 5 shows a high pass filter circuit which is operating in 5 kHz with C_1 = 100 nF and R_1 = 1.5 kΩ.

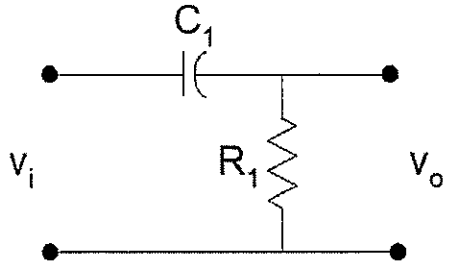

Figure 5

(i) Calculate the cutoff frequency. (2 marks)

(ii) Calculate the percentage of tilt. (3 marks)

(iii) Calculate the gain, A_V in decibel (dB). (3 marks)

(iv) Sketch the frequency response and label its cutoff frequency. (2 marks)

(b) Figure 6 shows a class A amplifier circuit which provides 4 V peak signal to a 1 KΩ load. The transistor which has arbitrarily large β. Assume $V_{BE} = 0.7$ V, Calculate the following:

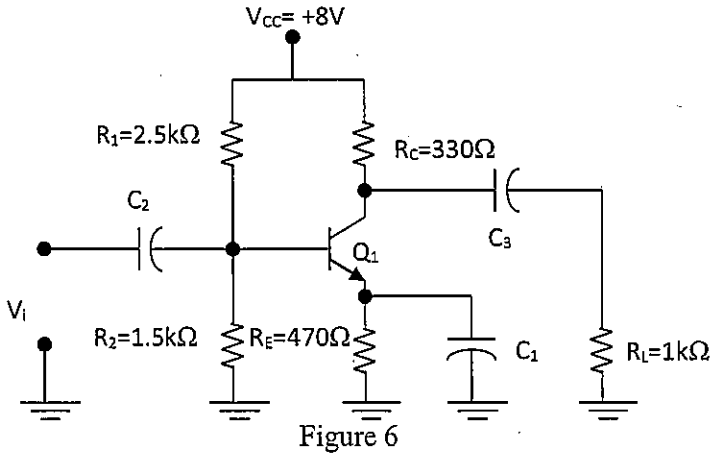

Figure 6

(i) Output power (2 marks)
(ii) Power efficiency (8 marks)

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(c) Figure 7 shows an astable multivibrator using a 555IC which produces 5 kHz output with 85% duty cycle. Assume $C_1 = 100$ nF. Determine the following:

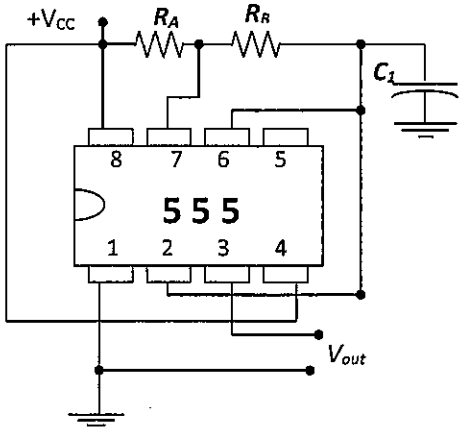

Figure 7

(i) R_A and R_B (6 marks)

(ii) Based on the answer of the (i), calculate the pulse width and space width. (4 marks)

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